ROUNISH CHANDRA

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ABOUT ME

I am a student of Electronics and Communication Engineering who is passionate about hardware innovation and digital systems. Skilled in VLSI design, verification, and performance analysis, with hands-on expertise in C, C++, Python, Verilog, and industry-standard tools. I am collaborative, adaptable, and driven to develop reliable, optimized solutions for real-world challenges.

EDUCATION

National Institute of Technology, Jalandhar **August 2025 - Present**
M.Tech. in Signal Processing & Machine Learning (ECE) CGPA: 7.97
Indian Institute of Information Technology, Dharwad **2021-2025**
B.Tech. in Electronics and Communication Engineering CPI: 8.03

SKILLS

Digital Logic & VLSI Design: Verilog, Synopsys DC, ICC2, PrimeTime, RTL coding, place & route, digital timing analysis
Embedded & Firmware: C, Embedded C, Python, Assembly, Arduino, low-power protocols (SPI, I2C, UART), RTOS
System Design: Microprocessor/SoC architecture, power management strategies, hardware-software co-design
Other: Analog electronics, IoT, simulation/emulation tools, collaborative product development

EXPERIENCE

Hardware Engineer Intern (Microsoft) **June 2026 – July 2026**

- **Developed a C-based CLI utility** for monitoring battery, thermal, and system-level statistics, strengthening expertise in C programming, memory management, debugging, parsing, and performance instrumentation.
- **Built GHOST (Geo-aware Human Optimized Safe Travel)** during the Microsoft Innovation Studio Hackathon, delivering an intelligent travel-safety solution using location-aware decision making and workflow automation.
- **Engineered a schema-driven CPER parsing framework in Python** to decode raw Common Platform Error Records (CPER) into structured JSON using GUID-based schema registries, binary data interpretation, and automated error analysis techniques.
- **Delivered an SDK Agent validation automation playbook** capable of validating all BMC function sensor-group test cases, including corner cases and edge conditions. Improved validation coverage and platform reliability by identifying, reproducing, and fixing bugs uncovered during test execution.

PROJECTS

Chip tapeout of SIDHARUD1*(inhouse project by IIITDharwad)* **June 2025 – July 2025**

- Helped design and test a custom port extender chip with a lot of features before it was made out of silicon. Used VLSI, digital logic, and the RISCV microprocessor to make and test a chip that extends a port. Led the pre-silicon verification and RTL integration of I2C, SPI, and UART peripherals, with a focus on making systems that use less power.

Object Detection Using Spiking Neural Network (*Object detection & hardware implementation)*
January 2025–April 2025

- Built a low-power Spiking Neural Network for FPGA object detection, applying digital verification, testbench automation, and ONNX quantization to enhance energy efficiency in embedded systems.

UAV based autonomous route mapping*(Image processing)* **August 2024–December 2024**

- Programmed UAVs to execute autonomous missions using embedded C and Python, conducted image processing with Pix4D, and post-processed spatial data with QGIS.

Crop Growth Monitoring System *(IoT Power Management)* **January 2024–April 2024**

- Created an agricultural hardware solution that is IoT-based and employs low-power microcontrollers and sensors to facilitate energy-efficient monitoring. Utilized power-aware transmission protocols (Blynk) and advanced control logic optimization techniques to optimize resource efficiency and decrease overall energy consumption.

RESPONSIBILITIES HIGHLIGHT *(From contributing Experience)*

- Assisted in formal pre-silicon verification, simulation, and emulation-based testbench development for digital subsystems
- Collaborated in multidisciplinary product teams, contributed to performance instrumentation, and participated in logic, timing, and verification cycles
- Received certification for Drone Workshop **(CDAC Bengaluru, Feb 2024)**